# SSC8122GS7

## N-Channel Enhancement Mode MOSFET with ESD Protection

### ➢ Features

| VDS | VGS | RDSON Typ. | ID | ESD |
|---|---|---|---|---|
| 20V | ±8V | 220mR@4V5 | 1.5A | 2K |
| | | 300mR@2V5 | | |
| | | 460mR@1V8 | | |

### ➢ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

### ➢ Applications

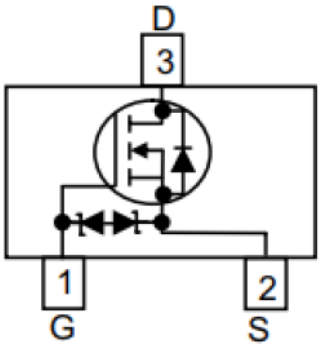
- Replace Digital Transistor
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching cell Phones

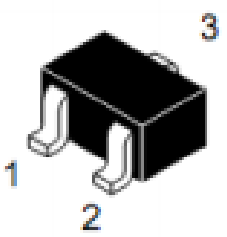
### ➢ Ordering Information

| Device | Package | Shipping |
|---|---|---|
| SSC8122GS7 | SOT323 | 3000/Reel |

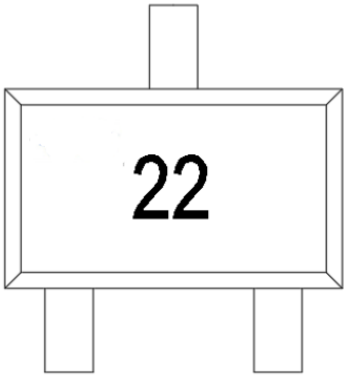
### ➢ Pin configuration

Top view




SOT323




Marking

## ➢ Absolute Maximum Ratings($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | 20 | V |
| $V_{GSS}$ | Gate-to-Source Voltage | ±8 | V |
| $I_D$ | Continuous Drain Current [a] | 1.5 | A |
| $I_{DM}$ | Pulsed Drain Current [b] | 4.5 | A |
| $P_D$ | Power Dissipation [c] | 0.46 | W |
| $P_{DSM}$ | Power Dissipation [a] | 0.25 | W |
| $T_J$ | Operation junction temperature | -55 to 150 | ℃ |
| $T_{STG}$ | Storage temperature range | -55 to 150 | ℃ |

## ➢ Thermal Resistance Ratings($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Typical | Maximum | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance [a] | | 500 | ℃/W |
| $R_{\theta JC}$ | Junction-to-Case Thermal Resistance | | 270 | |

Note:

a. The value of RθJA is measured with the device mounted on 1 $in^2$ FR-4 board with 2oz.copper,in a still air environment with TA=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

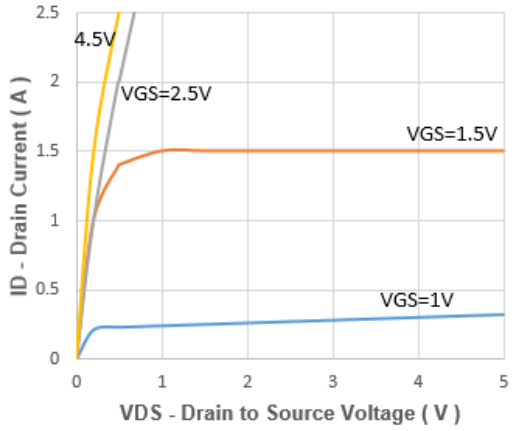
b. Repetitive rating, pulse width limited by junction temperature.

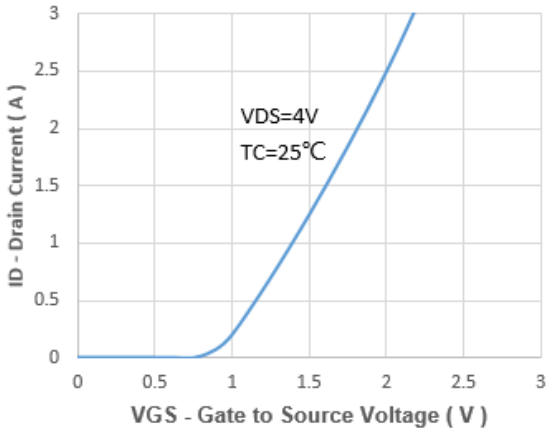
c. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

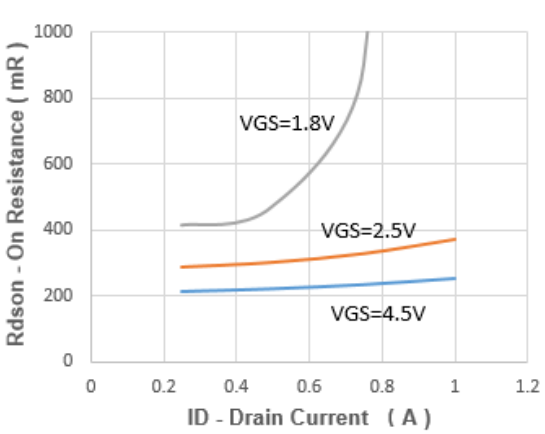
➢ **Electronics Characteristics**($T_A$=25℃ unless otherwise noted)

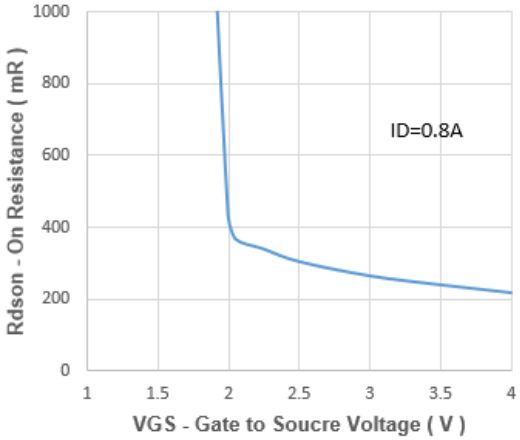
| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | VGS=0V,ID=250uA | 20 | | | V |
| $V_{GS\ (th)}$ | Gate Threshold Voltage | VDS=VGS,ID=250uA | 0.5 | 0.8 | 1.2 | V |
| $R_{DS(on)}$ | Drain-Source On-Resistance | VGS=4.5V,ID=0.55A | | 220 | 400 | mR |
| | | VGS=2.5V,ID=0.45A | | 300 | 500 | |
| | | VGS=1.8V,ID=0.35A | | 460 | 800 | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | VDS=16V,VGS=0V | | | 1 | uA |
| $I_{GSS}$ | Gate-Source leak current | VGS=±8V,VDS=0V | | | ±10 | uA |
| $G_{FS}$ | Forward Transconductance | VDS=5V,ID=0.45A | | 1.8 | | S |
| $V_{SD}$ | Forward Voltage | VGS=0V,IS=0.5A | | | 1.3 | V |
| Ciss | Input Capacitance | VDS=10V, VGS=0V, f=100KHZ | | 56 | | pF |
| Coss | Output Capacitance | | | 15 | | |
| Crss | Reverse Transfer Capacitance | | | 9 | | |
| $T_{D(ON)}$ | Turn-on delay time | VGS=4.5V, VDD=10V, RG=6R, ID=0.55A | | 22 | | ns |
| $T_{D(OFF)}$ | Turn-off delay time | | | 36 | | |

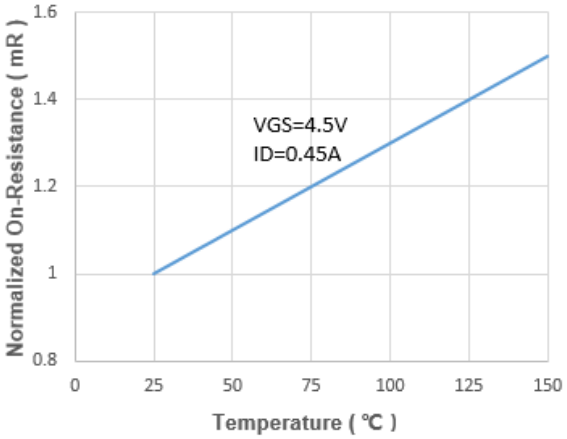
➢ **Typical Characteristics**($T_A$=25℃ unless otherwise noted)



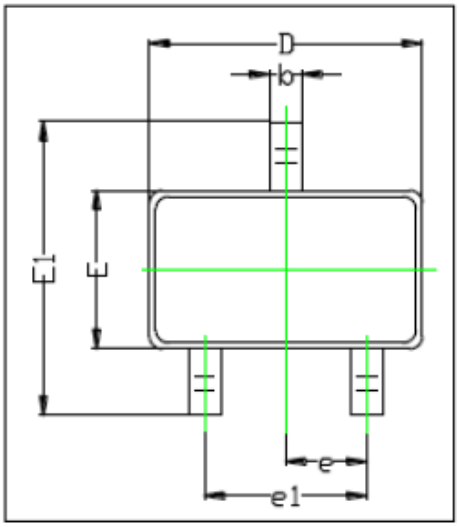



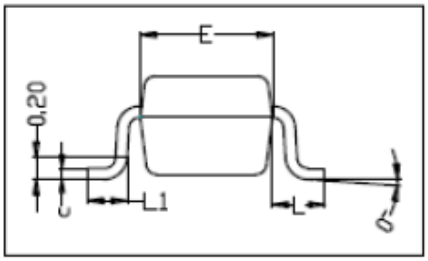



## ➢ Package Information

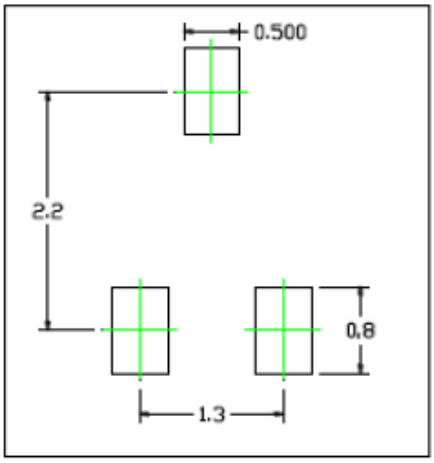
TOP VIEW



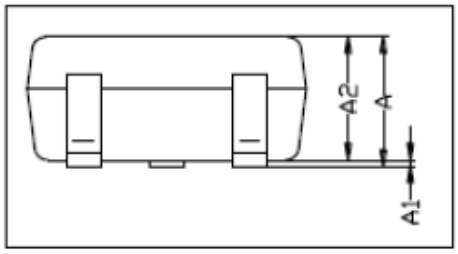

SIDE VIEW




SOLDERING PATTERN




FRONT VIEW




| SYMBOL | DIMENSIONS IN MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.900 | 1.000 |
| A1 | 0.00 | 0.100 |
| A2 | 0.900 | 1.000 |
| b | 0.200 | 0.400 |
| c | 0.080 | 0.150 |
| D | 2.000 | 2.200 |
| E | 1.150 | 1.350 |
| E1 | 2.150 | 2.450 |
| e | 0.650 TYP. | |
| e1 | 1.200 | 1.400 |
| L | 0.525 REF. | |
| L1 | 0.260 | 0.460 |
| θ | 0° | 8° |

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